

New non-volatile Logic based on Spin-MTJ

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Spin Transfer Torque (STT) writing approach based Magnetic Tunnel Junction (Spin-MTJ) (Fig.1) is excellent candidate to be used as Spintronics device in Magnetic RAM (MRAM) [1] and Magnetic Logic [2]. This effect was predicted by Slonczewski and Berger [3] in 1996, which shows that the spin magnetization in the storage layer of MTJ could be changed by flowing through a spin polarized current and the critical switching mechanism depends on the current density value. This critical current density has been found lately as low as 8×10^5 A/cm² [4] in Co₄₀Fe₄₀B₂₀/MgO/Co₄₀Fe₄₀B₂₀ stack structure; and as the dimension of Spin-MTJ is very small (e.g.113nm×75nm), the critical current could be thereby less than 150uA and easily generated by a small CMOS current source.

We have investigated two non-volatile logic circuits based on Spin-MTJ for Field Programmable Gate Array (FPGA) and System on Chip (SOC). The first one is a Spin-MTJ based non-volatile Look Up Table (Spin-LUT) (Fig.2). Working as a programmable and reconfigurable logic function generator, it memorizes all the configuration data in the MTJ arrays; and thus allows the FPGA logic circuit to reduce significantly its start-up latency from some microseconds down to some nanoseconds. It also allows realizing a sub-ns dynamical reconfiguration of the LUT during the signal processing. Spin-LUT non-volatile logic circuit has great potential in the field of complex logic digital system such as high performance game console and radar signal processing. The second one is Spin-MTJ based non-volatile Flip-Flop (Spin-FF) (Fig.3), data register and synchronizer, it stores permanently all the intermediate data processed in the FPGA or SOC circuit, thereby improves the data security and enable the complex logic system to restart immediately. Spin-FF could be advantageously used in the field of aviation and space where the security of data is one of the most important considerations. The lower critical current of STT writing approach makes these logic circuits work in less power and occupy smaller chip surface than with other writing techniques. Therefore the reduction of critical current has a strong impact on the performance of these Spin-MTJ based non-volatile logic circuits.

Another advantage of Spin-MTJ technology is that the storage element does not take much die area, because it is processed over the chip surface (see Fig.4). By using STMicroelectronics 90nm CMOS technology and a behavior Spin-MTJ simulation Model [5], Spin-LUT and Spin-FF have been demonstrated that they could work with high speed performance and small layout surface (Fig.5).

References:

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- [2] W.Zhao et al, "Integration of Spin-RAM technology in FPGA circuits" 8th International Conference on Solid-State and Integrated Circuit Technology, China, pp.799-802, 2006.
- [3] J.C.Slonczewski et al, "Current-driven excitation of magnetic multi-layers", Journal of Magnetism and Magnetic Materials, Vol159, pp.1-7, 1996.
- [4] J.Hayakawa et al, "Current-driven magnetization switching in CoFeB/MgO/CoFeB magnetic tunnel junctions", Japanese Journal of Applied Physics, 2005, Vol44, pp. 267-1270.
- [5] W.Zhao et al, "Macro-model of spin-transfer torque based Magnetic Tunnel Junction device for hybrid Magnetic-CMOS design", IEEE International Behavioral Modeling and Simulation Workshop, USA, pp. 40-43, 2006.

Figures:

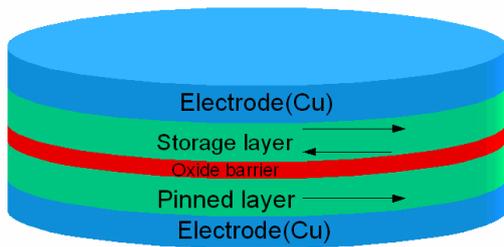


Fig.1 Magnetic Tunnel Junction is composed of three principle layers: an oxidation barrier, such as MgO and AlxOy; a Pinned layer and a storage layer, which are ferromagnetic Materiaux (e.g. CoFe). The spin direction in pinned layer is fixed, but can be changed in the storage layer, there are so that two states of MTJ: parallel and anti-parallel when the spin magnetization in pinned layer and storage layer is in the same direction or the opposite direction. For Spin Transfer Torque (STT) switching approach, the two MTJ states are decided by the critical current density I_c .

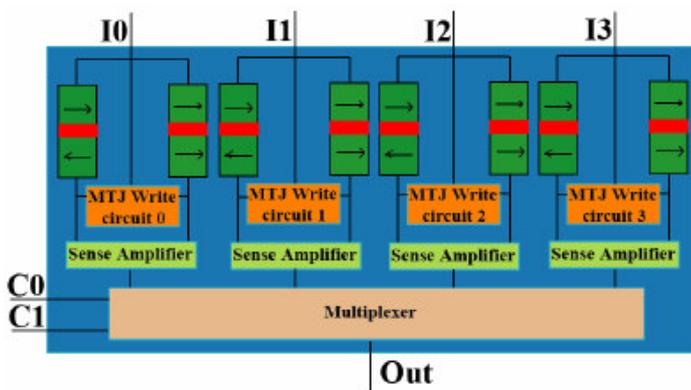
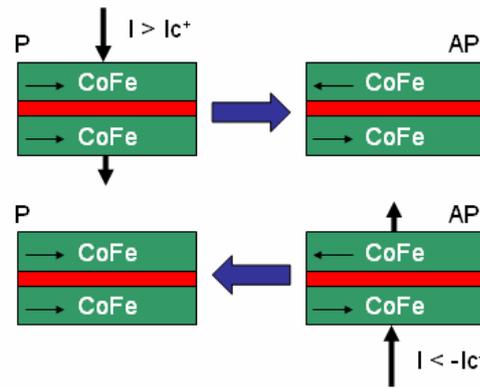


Fig.2 2-input Spin-LUT architecture

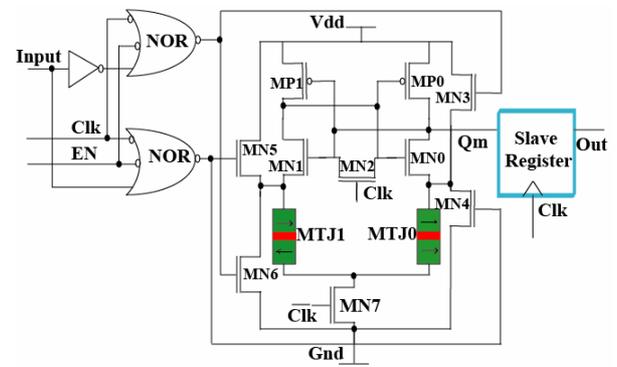


Fig.3 the full schematic of Spin-MTJ based Non-Volatile Flip-Flop (Spin-FF)

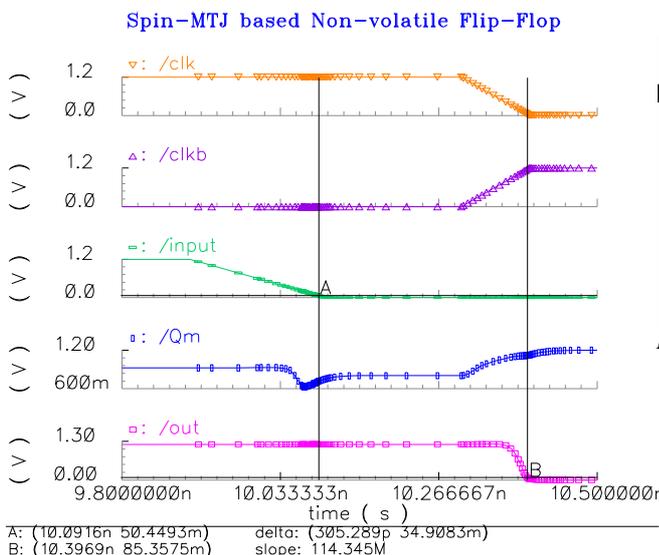


Fig.5.1 Simulation of Spin-FF, the points show that the propagation delay is about 300 ps

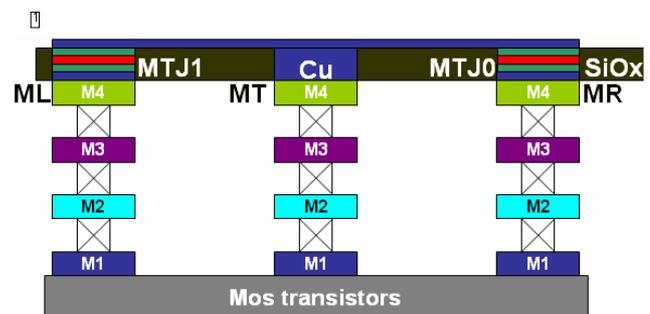


Fig.4 MTJ memory cells are implemented above the CMOS circuits

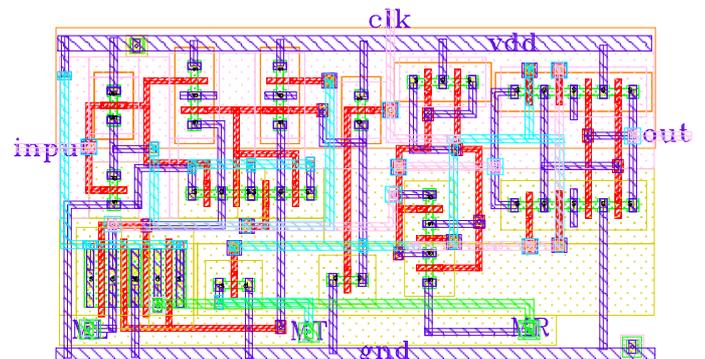


Fig.5.2 Full layout (5.65umx10.15um) of Spin-FF, MTJs are placed above the two points ML and MR, see also Fig.4