High Frequency Epitaxial Graphene Fields Effect Transistors (GFET) on SiC.

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Abstract

Since 2004, graphene has generated considerable interest in Physics. This revolutionary material for which discovery Novoselov's group in Manchester [1] received the Nobel Prize in Physics (2010) can be described as a two-dimensional single layer carbon crystal, arranged on a honeycomb lattice. It comprehends unique characteristics relevant to many researchers in various domains, especially in microelectronics for its potentially high carrier mobility even at room temperature. Owing to its 2D lattice, graphene is considered a semimetal -its band gap and its density of state (DOS) at Fermi level are both nil. Moreover at K and K' point the dispersion relation is linear and electrons are thus considered as relativistic massless particles and can theoretically reach a electron mobility of 100,000 cm²/V.s [1], [2].

In order to process devices on full wafer and pave the way for industrial graphene based transistors, we have decided to work on epitaxial graphene growths by thermal decomposition of Si-face silicon carbide. This sample was produced by the Laboratory for Photonics and Nanostructures (LPN CNRS). The graphene layer is characterized by a mapping of the full width at half maximum 2D Raman peak (FWHM) and shown in figure 1. The sample is estimated to be composed of a full mono or bilayer of graphene.

Based on the technological process describe in [3], top-gated epitaxial graphene field effect transistor (GFET) on SiC substrate (shown in figure 2) are patterned by successive steps of electron beam lithography and standard lift-off process with Ni/Au (50 / 300nm) ohmic contacts. After protecting the full active area with a negative hydrogen silsesquioxane (HSQ) resist, the excess of graphene surface was then etched by O_2 RIE.

The improvement of gate oxide quality was also a challenge in this work. We decided to use Al_2O_3 deposit by an Atomic Layer Deposition technique. To achieve a uniform deposition of this oxide on the hydrophobic surface of the carbon crystal [4], [5], we had to deposit by evaporation thin aluminium as seed layer (~2nm) which is oxidized in ambient before ALD.

Static measurements show the transfer characteristics and the Dirac point (on the figure 3) of a device at low V_{DS}. Due to the interaction with the substrate, the Dirac point is shifted to a negative V_{GS}. Drain current versus source-drain voltage described by the figure 4 doesn't show saturation characteristics, this is due to the semi-metal behavior of graphene. S parameters measurements were performed in microwave range from 250MHz to 40GHz on a Agilent E8361A. In order to obtain the extrinsic parameters, the influence of parasitic capacitances is removed from the *S* parameters measurements with an "open" deembedding structure which only includes the pads and the coplanar accesses of the device [6]. Extrinsic cut-off frequency (f_{t_extr}) has been extracted from H_{21_extr}. We report high frequency performances with an extrinsic cut-off frequency of 25GHz and the maximum oscillation frequency 19GHz at V_{DS}=3V and V_{GS}=-2.8V for a transconductance Gm=275mS/µm (see figure 5).

References

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Figures

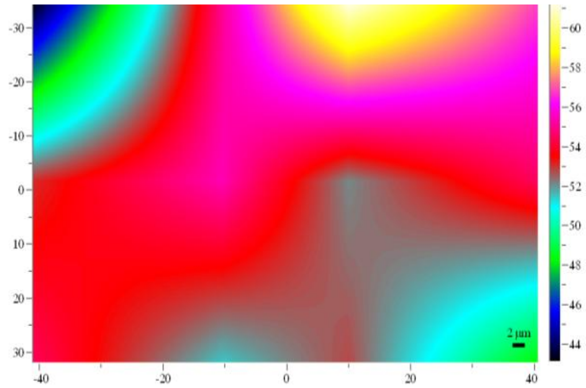

Figure 1: FHMW Raman mapping of epitaxial graphene on SiC (sample #G129).

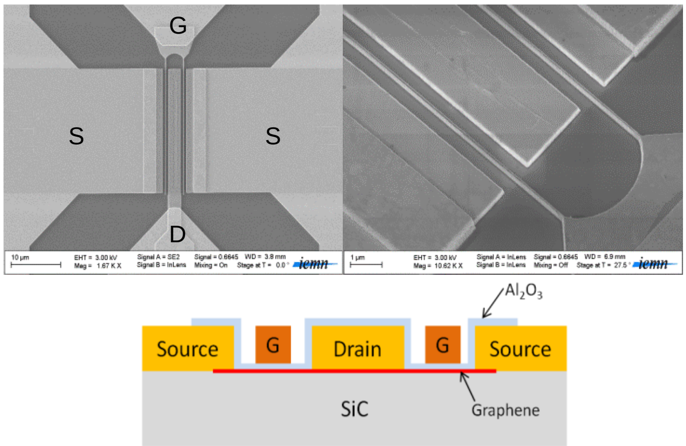

Figure 2 : SEM of one final GFET device.

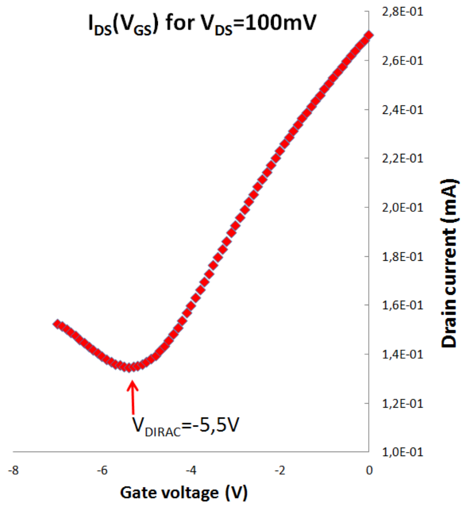

Figure 3: Dirac point voltage extracted from drain current versus gate voltage for a small V_{DS}=100mV.

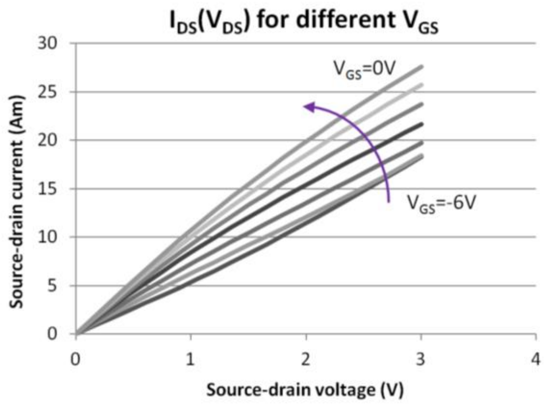

Figure 4: Measured output characteristics (drain current versus source-drain voltage) of a graphene transistor (L_G = 100 nm, W_{DS}=12µm and L_{DS}=0.6µm) for various top-gate voltages. (from -6V to 0V).

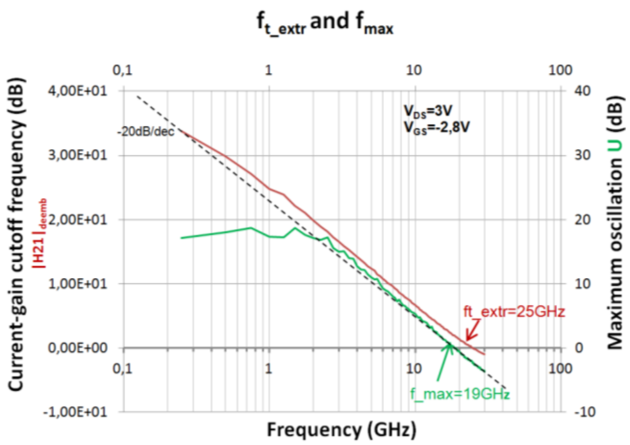

Figure 6: HF characteristics of GFET for L_G = 100 nm, W_{DS}=12µm and L_{DS}=1.1µm. Extrinsic $|H21|_{extrinsic}$ (red line) and maximum oscillation gain (green line) for V_{DS}=3V and V_{GS}=-2.8V. The dashed lines correspond to the ideal slopes of -20 dB/decade for |H21|.