# *Design of High-speed low power Reversible Logic BCD Adder Using HNG gate*

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Abstract - **Reversibility plays a fundamental role when computations with minimal energy dissipation are considered. In recent years, reversible logic has emerged as one of the most important approaches for power optimization with its application in low power CMOS, optical information processing, quantum computing and nanotechnology. This research proposes a new implementation of Binary Coded Decimal (BCD) adder in reversible logic. The design reduces the number of gate operations compared to the existing BCD adder reversible logic implementations. So, this design gives rise to an implementation with a reduced area and delay. We can use it to construct more complex systems in nanotechnology.**

*Keywords: BCD adder, decimal arithmetic, reversible logic, garbage output, HNG gate.*

## I. INTRODUCTION

Energy loss during computation is an important consideration in low power digital design. Landauer's principle states that a heat equivalent to kT*ln2 is generated for every bit of information lost, where 'k' is the Boltzmann's constant and T' is the temperature [1]. At room temperature, though the amount of heat generated may be small it cannot be neglected for low power designs. The amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Bennett showed that energy dissipation would not occur if the computations were carried out using reversible circuits [2] since these circuits do not lose information. A reversible logic gate is an n-input, n-output (denoted as n*n) device that maps each possible input pattern to a unique output pattern. There is a significant difference in the synthesis of logic circuits using conventional gates and reversible gates. While constructing reversible circuits with the help of reversible gates fan-out of each output must be 1 without feedback loops. As the number of inputs and outputs are made equal there may be a number of unutilized outputs called garbage in certain reversible implementations. This is the number of outputs added to make an n-input k-output function reversible.

For example, a single output function of 'n' variables will require at least n-1 garbage outputs. Classical logic gates such as AND, OR, and XOR are not reversible. Hence, these gates dissipate heat and may reduce the life of the circuit. So, reversible logic is in demand in power aware circuits.

A reversible conventional BCD adder was proposed in [4] using conventional reversible gates. In [4], a full adder design using two types of reversible gates - NG (New Gate) and NTG (New Toffoli Gate) with 2 garbage outputs was implemented. The BCD adder was then designed using such full adders. Even though the implementation was improved in [5] using TSG reversible gates, this approach was not taking care of the fanout restriction of reversible circuits, and hence it was only a near-reversible implementation. An improved reversible implementation of decimal adder with reduced number of garbage outputs is proposed in [6]. Another improved reversible implementation of decimal adder using reversible gates which results in further reduction in number of gates and garbage outputs with a fanout of 1 is proposed in [7]. The present work proposes a modified version of decimal addition using reversible gates which results in reduction in number of gate operations in full adder reversible gates with a fanout of 1. The design is done using 3 types of reversible gates.

The organization of this paper is as follows: Initially, necessary background on reversible logic gates that are used for the design is given. Then the proposed BCD adder is implemented using reversible gates. Finally, the paper concludes with a comparison of the proposed design with different types of reversible BCD adders available in literature, in terms of delay, number of gates and garbage outputs.

## II. REVERSIBLE LOGIC GATES

This section describes reversible gates that are used for the implementation of the proposed BCD adder.

Figure 1 shows a 3*3 New Gate [7]. New Gate can be used as a gate that generates an AND gate, an OR gate or an XOR gate. If B='0', then Q=C and R= (A'C')+ l=A+C.

Similarly, when C='0', then Q=AB and R=A+ B which are the carry and sum outputs of a half adder. Figure 2 shows a Feynman Gate [8]. Feynman Gate (FG) can be used as a copying gate. Since a fanout greater than one is not allowed, this gate is useful for duplication of the required outputs.

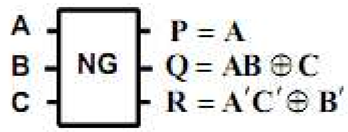


Figure 1: 3*3 New Gate (NG)

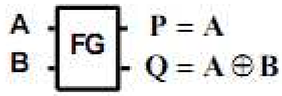


Figure 2: 2*2 Feynman Gate (FG)

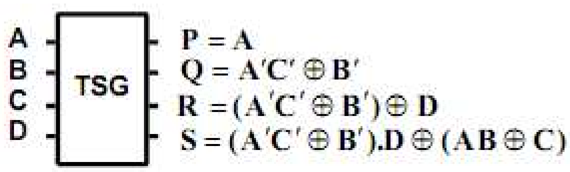


Figure 3: 4*4 TS Gate (TSG)

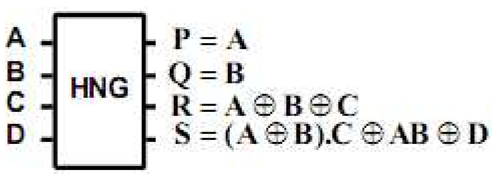


Figure 4: 4*4 HN Gate (HNG)

If B='0', then P=A and Q=A. Figure 3 shows a TS Gate (TSG) [9]. A full adder circuit can be realized by a TSG with C='0' and A, B and $C_{in}$ at A, B, D inputs of TSG. Then Sum and $C_{out}$ are realized at R and S outputs of TSG. A full adder circuit can also be realized by a HN gate (HNG)[3] shown in figure 4 with D='0' and A, B and $C_{in}$ at A, B, C inputs of HNG. Then Sum and $C_{out}$ are realized at R and S outputs of HNG.

## III. REVERSIBLE LOGIC IMPLEMENTATION OF DECIMAL ADDER

The BCD adder shown in Figure 5 has three blocks - 4-bit binary adder, 6-correction circuit and a modified special adder. 4-bit full adder adds the BCD inputs and generates a binary sum, S ($S_{3-0}$).This output is checked for a value greater than '9' or for a carry out, by the 6-correction circuit which generates a '6-correction' bit, 'L' using Equation (1).

$$L=C_{out} + S_3 (S_1+S_2) \qquad (1)$$

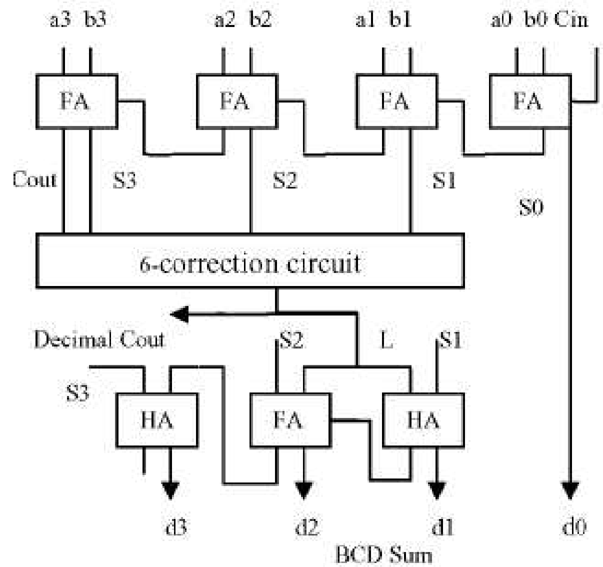


Figure 5: BCD Adder

The inputs to the second adder stage are S ($S_{3-0}$) and 4-bit number N ($N_{3-0}$) whose value is 6 ($0110_2$) or 0 ($0000_2$) depending on 'L' bit. So, $N_0$ and $N_3$ are always zero, and $N_1$ and $N_2$ is 'L' bit. To reduce the hardware and to increase the speed of the circuit, the final adder stage (special adder) is a modified version of the 4-bit binary adder with two half adders and one full adder.

Recently, reversible implementations of conventional BCD adders were proposed by Hafiz [4] Thapliyal [5] and James [6]. Implementation by Hafiz [4] makes use of 23 reversible gates and produces 22 garbage outputs whereas the implementation of Thapliyal [5] uses 11 reversible gates and produces 22 garbage outputs without taking care of fanout. There are 4 outputs in which the fanout is more than one in the implementation of [5], of which 3 are having fanout of 2 and the other having 3. If the fanout points were replaced by copying gates FG then the total number of gates would be increased to 16. Reversible implementation of BCD adder in [6] reduces the number of gates to 11 and garbage outputs to 13 with fanout restrictions. Reversible implementation of the BCD adder [10] uses the reversible gates such as TSG, FG and NG shown in Figure 5 takes care of the fanout restriction of reversible circuits and reduces the number of reversible gates. The proposed reversible implementation of the BCD adder done using the reversible gates such as HNG, FG and NG shown in Figure 7 also takes care of the fanout restriction of reversible circuits and reduces the number of reversible gate operations.

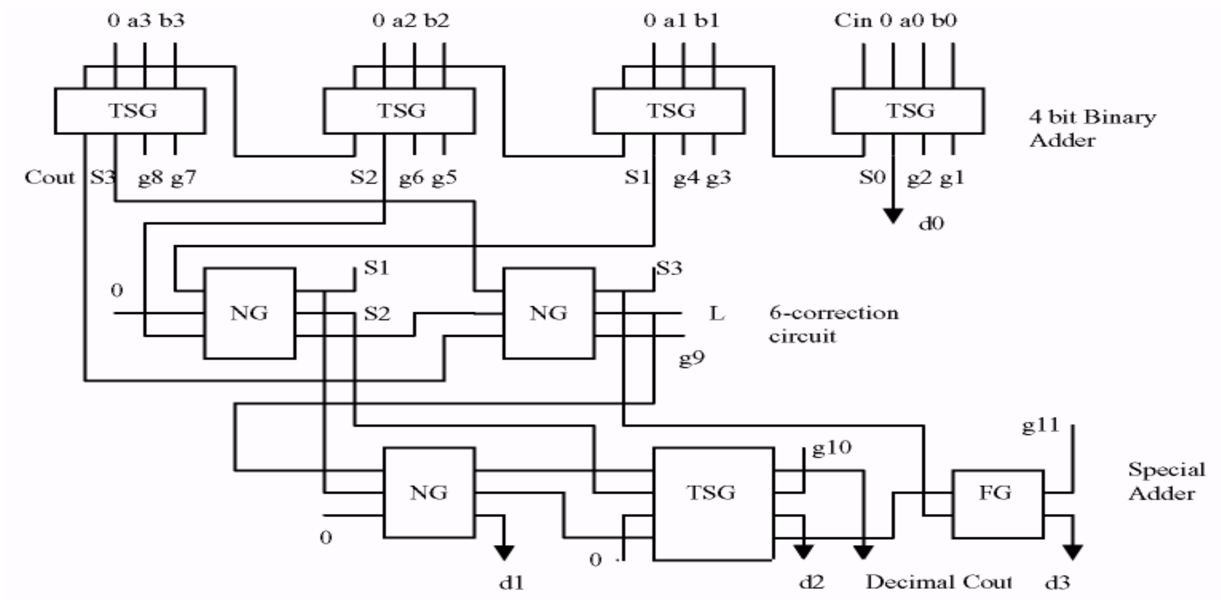


Figure 6: Reversible Implementation of BCD Adder in [10].

A 4-bit binary adder is implemented using 4 full adders. A full adder has 3 inputs and 2 outputs. To make a full adder reversible some garbage outputs are to be added. A reversible full-adder circuit can be realized with at least two garbage outputs. In full-adder circuit, there are three input combinations (0, 0, 1), (0, 1, 0) and (1, 0, 0) for which the output is same (1, 0). So, at least two garbage bits are required to make a unique output combination for each input combination. A number of reversible full adders are available in literature [7, 9]. But the implementation of a full adder using TSG [5] takes least number of gates, and produces least number of garbage outputs. Since a full adder can be implemented using one TSG, a 4-bit binary reversible adder implementation requires 4 TSGs and produces 8 garbage outputs. For reducing the number of gates, the 6-correction circuit output 'L' can be modified as in Equation (2).

$$L = Cout + S_3 (S_1+S_2) = Cout \oplus S_3 (S_1+S_2) \qquad (2)$$

It can be seen that the implementation requires 2 gates (2 NGs) to produce the 6-correction output, 'L', and the sum outputs ($S_{3\_1}$) with only one garbage output. The $S_1$, $S_2$ and $S_3$ outputs produced without using any copying gate (FG) can be used as inputs for the next stage. This gives a reduction of 3 gates and 4 garbage outputs compared to the implementation in [4].

Special adder is implemented using 3 gates (NG, HNG, FG). It is already seen that a 3*3 NG can implement a half adder, and a 4*4 HNG can implement a full adder. An FG replaces the final half adder in the special adder.

This is because only the sum bit ($d_3$) is required as decimal sum output and the carry is discarded from the final addition. So, using an NG will give rise to 2 garbage outputs while an FG will produce only one garbage output. The BCD sum is indicated as $d_{3\text{-}0}$ carryout from the stage as 'Decimal $C_{out}$ in Figure 6. This implementation uses 9 reversible gates, and produces 11 garbage outputs. Further, it is noted that the implementation in [4] can be used only as a single digit BCD adder since a carryout (Decimal $C_{out}$) is not produced. This may be resolved by the addition of one more copying gate. The proposed design shown in Fig 7 can be used for cascading BCD adders for multidigit BCD addition with the help of the carry out (Decimal $C_{out}$) produced.

An N-digit BCD adder will have a total (worst case) delay (dsum) equal to the sum of the 'carry delay' ($T_{dcout}$) through N digits and 'sum delay' through the last digit ($T_{sum\cdot digit}$).this is given in equation (3).

$$T_{dsum} = NTd_{cout} + T_{special\ adder} \qquad (3)$$

Where Tdout=($T_{bin\text{-}adder}$+$T_{6\text{-}correction}$).

$T_{bin\text{-}adder}$ is the delay of 4-bit binary adder.

$T_{6\text{-}correction}$ is the delay in generating decimal $c_{out}(d_{cout})$ after $T_{bin\text{-}adder.}$

$T_{special\text{-}adder}$ is the additional delay of the final adder stage (special adder) of the last digit after generating Decimal $c_{out}(d_{cout})$.

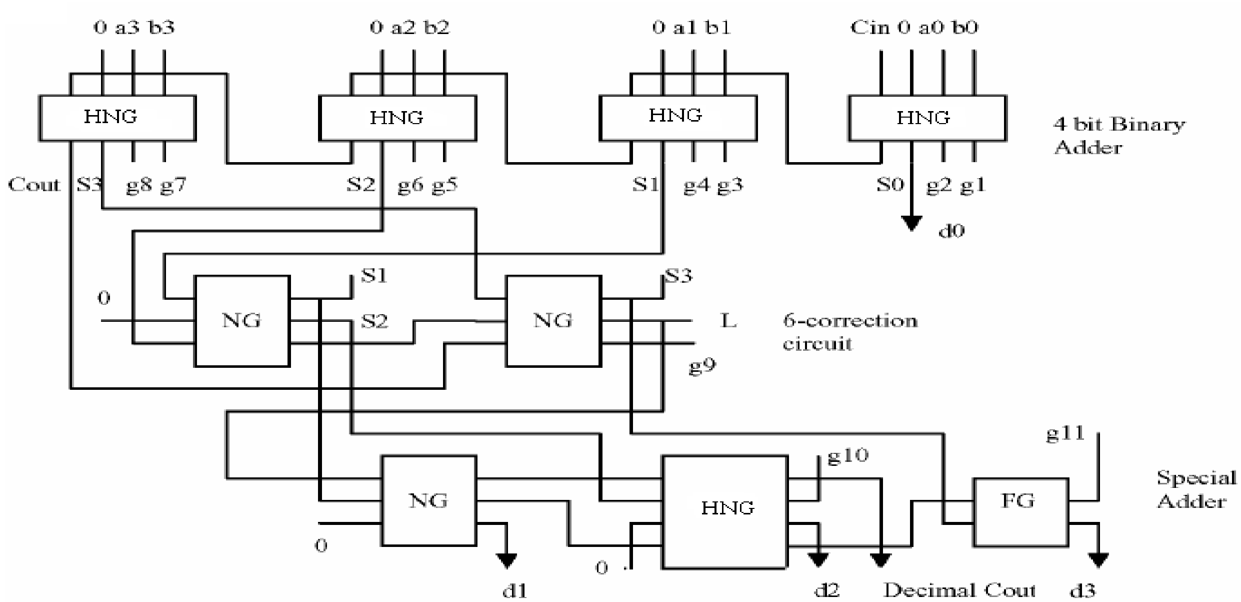


Figure 7: Proposed Reversible Implementation of BCD Adder.

TABLE 1. COMPARATIVE ANALYSIS OF REVERSIBLE BCD ADDERS

| Reversible BCD Adders | 4 bit Adder | | 6 -correction circuit | | Correction/ Special Adder | | Complete Circuit | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | No: of gates | No: of garbage o/p | No: of gates | No: of garbage o/p | No: of gates | No: of garbage o/p | No: of gates | No: of garbage o/p | Delay of Decimal Cout for N-digit BCD adder | Delay of BCD Sum for N-digit BCD adder |
| BCD Adder in [4] | NG-4 NTG-4 Total-8 | 8 | FG-3 NG-3 Total-6 | 6 | NG-4 NTG-4 Total-8 | 8 | NG-11 NTG-8 FG-3 Total-22 | 22 | 12N | 12N+7 |
| BCD Adder using TSG [5] (fanout>l | TSG-4 | 8 | NG-3 | 6 | TSG-4 | 8 | TSG-8 NG-3 Total- 11 | 22 | 7N | 7N+3 |
| BCD Adder using TSG [5] (fanout=l | TSG-4 | 8 | FG-3 NG-3 Total-6 | 6 | TSG-4 FG-2 Total-6 | 8 | TSG-8 NG-3 FG-5 Total- 16 | 22 | 9N | 9N+4 |
| BCD Adder in [6] (fanout=l | TSG-4 | 8 | NG-2 FG-1 Total-3 | 2 | FG-2 NG-1 TSG-1 Total-4 | 3 | TSG-5 NG-3 FG-3 Total- 11 | 13 | 7N | 7N+3 |
| BCD Adder In(10) (fanout=l | TSG-4 | 8 | NG-2 | 1 | FG-1 NG-1 TSG-1 Total-3 | 2 | TSG-5 NG-3 FG-1 Total-9 | 11 | 7N | 7N+1 |
| **Proposed BCD Adder (fanout=l** | **HNG-4** | **8** | **NG-2** | **1** | **FG-1 NG-1 HNG-1 Total-3** | **2** | **HNG-5 NG-3 FG-1 Total-9** | **11** | **7N** | **7N+1** |

For a reversible implementation this is given as

$$T_{rev\text{-}dsum}=7N+1 \qquad (4)$$

Where $T_{rev\text{-}dout}=T_{rev\text{-}bin\text{-}adder}+T_{rev\text{-}6\text{-}correction}$

$T_{rev\text{-}bin\text{-}adder} =$ 4 gate delays (4HNG)

$T_{rev\text{-}6\text{-}correction} =$ 3 gate delays (2NG+1HNG)

$T_{rev\text{-}bin\text{-}adder} =$ 1 gate delay (1FG)

Similar analysis done on reversible implementations of BCD adders in [4], [5] and [6] are tabulated in Table 1. Even though this delay analysis will not give exact results because of the difference in complexity of the gates used, it gives a good estimate of the delay reduction attained by reversible implementation of proposed BCD adder. The Table also shows a comparison in terms of number of reversible gates and garbage outputs at different levels and for the complete circuit. It is clear that the proposed implementation uses least number of gate operations and gives least delay compared to all other implementations. The reduction in number of gate operations (area) required will lead to reduced power consumption.

## IV. RESULTS AND DISCUSSION

Evaluation of the proposed reversible BCD adder circuit is: the proposed reversible adder circuit is more efficient than existing circuit presented in [10] evaluation of proposed circuit can be comprehended easily with the help of the comparative analysis in Table 2.

Table2: comparative experimental results of existing and proposed reversible adder circuits.

| Reversible BCD adder circuit | Total logical calculation (T) |
|---|---|
| Design in [10] | 27a+21b+24c |
| Proposed Design | 27a+16b+9c |

The only difference between proposed design with the existing design in [10] is the use of HNG gate instead of TSG gate. We use it because the HNG gates have less logical calculation than the TSG gates. One of the main factors of the circuit is its hardware complexity.

We can prove that our proposed circuit is better than the exiting approaches in terms of hardware complexity.

Let

a=A two input EX-OR gate calculation

b==A two input AND gate calculation

c=A NOT gate calculation

T=Total logical calculation

For [10] the total logical calculation is:

27a+21b+24c

For our proposed design logical calculation is:

27a+16b+9c

Therefore, the proposed reversible adder circuit is better than the existing circuits in terms of complexity.

## V. CONCLUSION AND FUTURE WORK

A modified reversible BCD adder implementation is presented. The architecture is specially designed to make it suitable for reversible logic implementation. It is demonstrated that the proposed design is highly optimized in terms of number of reversible gate operations.

The design strategy is chosen in such a way to reduce the most important factor of the reversible circuit cost: the number of reversible gate operations. This work forms an initial step in the building of complex reversible systems, which can execute more complicated operations. The reversible circuit proposed here forms the basis of a Decimal ALU for a reversible CPU. VLSI implementations using only one type of modular building block can decrease system design and manufacturing cost. Characterization of new families of 'n-input' - 'n-output' reversible gates that can be used for regular structures is an area which can be explored further. In this research, a known traditional logic implementation for BCD adder was modified to get a delay reduction for multi-digit addition, and then each of the internal elements was replaced with reversible equivalents. Further investigation into determining alternate implementations can be done using logic synthesis methods.

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